



## **INTRODUCTION**

SCT is a professional mixed mode IC design house. We aim to provide you the best ICs by executing an unbeatable quality controlling program of design and precise mass production flow. To assure greatest product reliability, SCT maintains and pursues a comprehensive reliability qualification program via various stress conditions of industrial standards, i.e. JEDEC-22B/JESD22-A. SCT's ultimate reliability monitoring program includes the following three main items:

- 1) ESD & Latch-up test (SCT)
- 2) Life and Environmental test (packaging house & SCT)  
Pre-condition, HTOLT, PCT, HAST, TCT
- 3) Mechanical (Packaging house)  
Solder-ability, Marking Permanency, Lead Integrity Test,  
Mechanical Shock, Physical Dimensions

The following test descriptions demonstrate SCT's common tests guideline and a robust check for device qualification and routine reliability monitoring.

## **RELIABILITY TEST DESCRIPTIONS**

### **Electrostatic discharge (ESD)**

Electrostatic discharge sensitivity tests are designed to measure the sensitivity of each device pin to electrostatic discharges that may occur during device handling. The Human Body Model (HBM) is to evaluate the immunity of ICs against static electricity discharge from human body when ICs are exposed during handling. It is based on a high-current pulse (positive and/or negative) of longer duration, simulating discharge through human contact. The Machine Model (MM) is to evaluate the immunity of ICs against static electricity discharge from machine when ICs are exposed during handling. It is based on a high-voltage short duration pulse (positive and/or negative) simulating a device pin coming in contact with a grounded surface.

### **Latch-up**

The Latch-up test is to evaluate the immunity of IC to "Latch-up", which is a temporary short-circuiting with high current between the power source and the ground caused by electric noise/spike coming from the pins of a device through two parasitic bipolar structures. In the case, current (positive and/or negative) is injected on individual input/output pins in junction to VCC & tested pin using VCC + 10% voltage stress while the power supply current is monitored.

### **High Temperature Operation Life Test (HTOLT)**

The High Temperature Operating Life test is used to thermally accelerate those wear out and failure mechanisms that would occur as a result of operating the device continuously in a system application. A pattern specifically designed to exercise the device at maximum operating voltage and the high temperature.

### **Highly Accelerated Stress Test (HAST)**

Highly Accelerated Stress Test (HAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Biased HAST test is used to accelerate threshold shifts in the MOS device associated with moisture diffusion into the gate oxide region as well as electrochemical corrosion mechanisms within the device package.

### **Temperature Cycling Test (TCT)**

Temperature cycling testing accelerates the effects that changes in temperature will cause between different components within the specific die and packaging system due to differing expansion coefficients. During test period, devices are inserted into a chamber where temperatures are rigidly controlled.

### **Pressure Cooker Test (PCT)**

Pressure cooker test accelerates the failure effects that device in high pressure and high moisture environment. That is qualified the capability of package moisture resistance. Typical examples of damage caused by this test include chip function failed by device characteristics change and metal corrosion.

### **Solder-ability**

The solder-ability test is used to determine the ability of package leads to be wetted by solder. This test verifies that the method of lead treatment to facilitate solder-ability is satisfactory and will allow successful solder connection to designated surfaces.

### **Mark Permanency**

The mark permanency test verifies package marking to solvents and cleaning solutions which is commonly used for removing solder flux on circuit boards to ensure the marking will not become illegible. Devices and a brush are immersed into one of four specified solvents for one minute then removed. The devices are then brushed ten strokes. This process is repeated three times for each group of solvents and devices. After rinsing and drying the devices, they are examined for legibility according to specified criteria.

### **Physical Dimensions**

The physical dimensions test verifies that all package dimensions fall within specified dimension ranges on the applicable package drawing. Equipment utilized for these measurements must have sufficient accuracy to determine actual device dimensions.

## Lead Integrity

The lead integrity test provides tests for determining the integrity of device leads, welds, and seals. Devices are subjected to various stresses including tension, bending fatigue and torque. Devices are then examined under magnification to determine any evidence of breakage, loosening or motion between the terminal and device body.

## Mechanical Shock

The mechanical shock test is intended to determine the suitability of the devices for use in electronic equipment which may be subjected to moderately severe shocks as a result of suddenly applied forces or abrupt changes in motion produced by rough handling, transportation, or field operation. Shocks of this type may cause damage similar to that resulting from excessive vibration, particularly if the shock pulses are repetitive.

## RELIABILITY QUALIFICATION

| Test Item           | Sample Size | Test Conditions  | Qualification Requirement  |
|---------------------|-------------|--|----------------------------|
| ESD - HBM           | 6           | > 3500V  | New process<br>New product |
| ESD - MM            | 6           | > 150 V  |                            |
| Latch-up            | 6           | > 150 mA/max. VCC  |                            |
| HTOLT-dynamic       | 26          | 125°C/max. VCC/1000 hours  |                            |
| Pre-condition       | 32          | TCT (5 cycles) + Bake (24 hrs /125°C) + Moisture Soak 30°C/ 60% RH /192hrs) + IR-reflow (3 cycles) |                            |
| High temp. storage  | 32          | 150°C/500 hours  |                            |
| Solder-ability      | 3           | Steam precondition 4~8hrs/245°C /5 secs  |                            |
| PCT                 | 32          | 121°C/100%RH168hrs   |                            |
| HAST                | 32          | 130°C/85%RH/168hrs   |                            |
| TCT                 | 32          | -65°C~150°C/500cycles, 15minutes/cycle   |                            |
| Thermal shock       | 15          | -65°C ~ 150°C/5min→3secs→5min / 500Cycles  | New process<br>New product |
| Ink mark permanency | 3           | Mark legible in one of 4 solutions. Monitor if mark is degrading.                                  | New package                |
| Physical dimensions | 5           | Package draw diagram   |                            |
| Lead integrity      | 3           | Refer to JEDEC-22B-105B  |                            |
| Vibration           | 15          | 20~1000 Hz for 10 min. 20g's for 4 min. in 3 planes  |                            |
| Mechanical shock    | 15          | Functional 1500gms for 5ms   |                            |

[\(check up-to-date version\)](#)